TEMPERATURE AND PROCESS INDEPENDENT CMOS CIRCUIT

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to analog circuits such as multipliers, adaptive filters, function generators, modulators, and neural networks. More particularly, this invention relates to compensation circuits incorporated with analog circuits to offset deviation in operation of the analog circuit due to variations in temperature and process.

2. Description of Related Art

Analog function circuits such as multipliers, adaptive filters, function generators, modulators, and neural networks, as is known in the art, produce a voltage output, which is proportional to an arithmetic function of two voltage inputs. As semiconductor processing has improved, more and varied circuits are formed on a semiconductor substrate. This has mandated the creation of libraries of analog function circuits or analog function cores. FIG. 1 shows a system diagram of an analog function core. There are two differential voltage inputs vx, vy, and one differential voltage output vout. A load resistor RL is connected between the inverted and non-inverted output the differential voltage output vout. The differential output voltage vout is developed across a load resistor, RL and is determined by the formula:

$$vout=kF(vx,vy) \quad \text{EQ. 1}$$

where:

k is a constant of proportionality or scaling factor.

F is the arithmetic function to be performed on the two differential input signals vx and vy.

The load resistor RL of FIG. 1 can be formed of the two load resistors RL1 and RL2 as shown in FIG. 2. The load resistor RL1 is connected between the inverting output (−) of the differential output voltage vout and the common mode biasing voltage source Vcm. The load resistor RL2 is connected between the non-inverting output (+) of the differential output voltage vout and the common mode biasing voltage source Vcm.

The voltage level present at the inverted (−) output terminal of the differential output vout is determined as:

vout−=Iout1*RL1+Vcm where:

I_{out1} is the output current and is determined as a function of the two differential input signals vx and vy.

RL1 is the resistance value of the load resistor.

Conversely, the voltage level present at the non-inverted (+) output terminal of the differential output vout is determined as:

vout+=Iout2*RL2+Vcm

where:

I_{out2} is the output current and is determined as a function of the two differential input signals vx and vy.

RL2 is the resistance value of the load resistor.

FIG. 3 shows an example of an analog function circuit implemented as a voltage multiplier with differential voltage inputs and a voltage output across a load resistor. The non-inverting input vx+ of the first differential voltage input vx is connected to the gate of one of the n-type metal oxide semiconductor (MOS) transistors M1 of a parallel connected pair of n-type MOS transistors M1 and M2. The gate of the second n-type MOS transistor M2 of the parallel connected pair of n-type MOS transistors M1 and M2 is connected to the inverting input vx− of the first differential voltage input vx. The commonly connected sources of the parallel connected pair of n-type MOS transistors M1 and M2 are connected to a first terminal of a current source Ib3. The second terminal of the current source Ib3 is connected to a ground reference point. The commonly connected drains of the parallel connected pair of n-type MOS transistors M1 and M2 are connected to a first terminal of a current source Ib1. The second terminal of the current source Ib1 is connected to a power supply voltage source V_{DD}. The junction of the commonly connected drains of the parallel connected pair of n-type MOS transistors M1 and M2 and the first terminal of a current source Ib3 form the output terminal containing the inverted output (−) of the differential output voltage vout.

The non-inverting input vy+ of the first differential voltage input vy is connected to the gate of one of the n-type metal oxide semiconductor (MOS) transistors M3 of a parallel connected pair of n-type MOS transistors M3 and M4. The gate of the second n-type MOS transistor M4 of the parallel connected pair of n-type MOS transistors M3 and M4 is connected to the inverting input vy− of the second differential voltage input vy. The commonly connected sources of the parallel connected pair of n-type MOS transistors M3 and M4 are connected to a first terminal of a current source Ib4. The second terminal of the current source Ib4 is connected to a ground reference point. The commonly connected drains of the parallel connected pair of n-type MOS transistors M3 and M4 are connected to a first terminal of a current source Ib2. The second terminal of the current source Ib2 is connected to a power supply voltage source V_{DD}. The junction of the commonly connected drains of the parallel connected pair of n-type MOS transistors M3 and M4 and the first terminal of a current source Ib2 form output terminal containing the non-inverted output (+) of the differential output voltage vout.

The load resistor RL1 is connected between the inverting output (−) of the differential output voltage vout and the common mode biasing voltage source Vcm. The load resistor RL2 is connected between the non-inverting output (+) of the differential output voltage vout and the common mode biasing voltage source Vcm.

The gates of the parallel connected pair of n-type MOS transistors M1 and M2 and the gates of the parallel connected pair of n-type MOS transistors M3 and M4 are biased externally with a constant voltage source VB (not shown) to cause the parallel connected pair of n-type MOS transistors M1 and M2 and the parallel connected pair of n-type MOS transistors M3 and M4 to operate in the saturation region. This insures that any voltage developed from the drains to the sources of the parallel connected pair of n-type MOS transistors M1 and M2 or the parallel connected pair of n-type MOS transistors M3 and M4 does not effect the saturation drain-to-source current Ids through the parallel connected pair of n-type MOS transistors M1 and M2 or the parallel connected pair of n-type MOS transistors M3 and M4.

The drain-to-source saturation current Ids_{sat} of each of the parallel connected pair of n-type MOS transistors M1 and M2 or the parallel connected pair of n-type MOS transistors M3 and M4 is found by the formula:

$$Ids_{sat}=K(VGS-VT)^2$$

where:

VGS is the gate-to-source of each MOS transistor.

VT is the threshold voltage at which MOS transistor begins to conduct or turn-on.

K is a process constant found as the function

$$K = \mu_s\left(\frac{C_{ox}}{2}\right)\left(\frac{W}{L}\right)$$

where:

μ_s is the mobility of the bulk doped semiconductor material that forms the channel.

C_{ox} is the capacitance of the gate oxide of the MOS transistors.

$$\left(\frac{W}{L}\right)$$

is the width-to-length ratio of the MOS transistors.

As can be shown from Einstein's Relationship, the mobility μ_s of the semiconductor material is dependent upon the absolute temperature of operation. Further, any changes in the process that effects the doping of the semiconductor material will further change the value of the mobility μ_s of the semiconductor material. Additionally, process changes may effect the geometric values of the width-to-length ratio

$$\left(\frac{W}{L}\right),$$

as well as the thickness of the insulating material that forms the gate oxide, which will change the values of the capacitance C_{ox}.

It can be shown that the output currents I_{out1} and I_{out2} can be calculated by the formula:

$$I_{out1} = I_{out2} = \mu_n(C_{ox})\left(\frac{W}{L}\right) * v_x * v_y$$

where:

μ_n is the mobility of the bulk doped semiconductor material that forms the channel.

C_{ox} is the capacitance of the gate oxide of the parallel connected pair of n-type MOS transistors M1 and M2 and the parallel connected pair of n-type MOS transistors M3 and M4.

$$\left(\frac{W}{L}\right)$$

is the width-to-length ratio of the parallel connected pair of n-type MOS transistors M1 and M2 and the parallel connected pair of n-type MOS transistors M3 and M4.

Thus, the voltage level present at the inverted (−) output terminal of the differential output vout is determined as:

$$Vout += I_{out1} * RL1 = \mu_n C_{ox}\left(\frac{W}{L}\right) * v_x * v_y * RL1 \quad \text{Eq. 3}$$

and the voltage level present at the non-inverted (+) output terminal of the differential output vout is determined as:

$$Vout -= I_{out2} * RL2 = \mu_n C_{ox}\left(\frac{W}{L}\right) * v_x * v_y * RL2. \quad \text{Eq. 4}$$

BRIEF SUMMARY OF THE INVENTION

An object of this invention is to provide an analog integrated circuit such as a multiplier, adaptive filter, function generator, modulator, or neural network whose output voltage signal is independent from variations in temperature and process.

Another object of this invention is to provide a compensation circuit in connection with or integrated with an analog circuit such as a multiplier, adaptive filter, function generator, modulator, or neural network to make the output signal of the analog circuit not vary with changes in temperature and manufacturing process.

To accomplish these and other objects a temperature and process independent analog integrated circuit has an analog integrated function core circuit. The function core circuit has a first differential pair of input terminals to receive a first input signal, a second differential pair of input terminals to receive a second input signal, and a differential pair of output terminals. The differential pair of output terminals contains an output signal that is a function of a scaling constant, the first input signal, and the second input signal.

The analog integrated circuit has a first and a second loading device. The first loading device has a first terminal connected to an inverted terminal of the differential pair of output terminals, a second terminal connected to a common mode voltage terminal, and a third terminal. A loading control voltage at the third terminal controls a loading on a voltage signal present at the inverted terminal by the first loading device. The second loading device has a first terminal connected to an non-inverted terminal of the differential pair of output terminals, a second terminal connected to the common mode voltage terminal, and a third terminal. The loading control voltage also at the third terminal controls the loading on a voltage signal present at the non-inverted terminal by the second loading device. The first and second loading devices in the preferred embodiment are MOS transistors of a second conductivity type and are biased by a loading device controller to operate in a linear operation region of the first and second loading devices.

The loading device controller within the analog integrated circuit compensates for changes in voltage level of the output signal due to variations in temperature and variations in manufacturing process within the function core circuit. The loading device controller has a loading control voltage terminal to provide the loading control voltage. The loading device controller has a first MOS transistor of a first conductivity type with a gate connected to a first control bias voltage source, a source connected to the ground reference point, and a drain. The loading device controller has a second MOS transistor of the first conductivity type with a source connected to the drain of the first MOS transistor of the first conductivity type, a gate, and a drain. A first MOS transistor of the second conductivity type has a source connected to the common mode voltage terminal, a drain connected to the second MOS transistor of the first conductivity type, and gate connected to the loading control voltage terminal. A first differential amplifier has an inverting input connected to a second control bias voltage source, a non-inverting input connected to the connection of the drain of the first MOS transistor of the second conductivity type and the drain of the second MOS transistor of the first conductivity type, and an output connected to the gate of the first MOS transistor of the second conductivity type and forms the loading control voltage terminal. The voltage present at the connection of the drain of the first MOS transistor of the second conductivity type and the drain of the second MOS transistor of the first conductivity type is maintained at a voltage level equal to a voltage level of the second bias control voltage source. A second differential amplifier has an inverting input connected to the connection of the drain of

the first MOS transistor of the first conductivity type and the source of the second MOS transistor of the first conductivity type, a non-inverting input connected to a third biasing control voltage source, and an output connected to the gate of the second MOS transistor of the first conductivity type. The voltage at the connection of the drain of the first MOS transistor of the first conductivity type and the source of the second MOS transistor of the first conductivity type is maintained at the voltage level of the third biasing voltage source.

Further, the analog integrated core circuit has a biasing circuit. The biasing circuit has the common mode voltage terminal to provide a common mode voltage to the first and second loading devices and in communication with the compensation circuit provide the first, second and third control bias voltage sources.

The bias circuit includes a bandgap referenced current source. The bandgap referenced current source provides a reference current that is independent of temperature. A current mirror has a reference terminal that is responsive to the reference current source, a first terminal coupled to the compensation circuit to provide a first current proportional to the reference current and second terminal to provide a second current proportional to the reference current.

The bias circuit has a first resistor connected to the first terminal of the current mirror. A threshold voltage generator is connected between a second terminal of the first resistor and a ground reference point such that the first bias voltage source is provided to the first to the compensation circuit.

A voltage divider is connected between the second terminal of the current mirror and the ground reference point. The voltage divider has a first terminal to provide the second bias voltage source to the compensation circuit and a second terminal to provide a third bias voltage source to the compensation circuit. A voltage buffer has an input terminal that is in communication with the connection of the second terminal of the current mirror and the voltage divider. An output terminal is connected to the common mode voltage terminal to provide the common mode voltage source in response to a fourth biasing voltage present at the connection of the second terminal of the current mirror and the voltage divider.

If the analog integrated core circuit is a multiplier circuit, it has a first and a second parallel connected pair of MOS transistors of a first conductivity type. A gate of one MOS transistor of the first parallel connected pair of MOS transistors is connected to an inverting input of the first differential pair of input terminals. A gate of the other MOS transistor of the parallel connected MOS transistors is connected to a non-inverting input of the first differential pair of input terminals. Commonly connected drains are connected to the inverted terminal of the differential pair of output terminals. Likewise, gate of one MOS transistor of the second parallel connected pair of MOS transistors is connected to an inverting input of the second differential pair of input terminals. A gate of the other MOS transistor of the parallel connected MOS transistors is connected to a non-inverting input of the second differential pair of input terminals. Commonly connected drains are connected to the non-inverted terminal of the differential pair of output terminals. A first biasing constant current source is connected between a power supply voltage source and the commonly connected drains of the first parallel connected MOS transistors, and a second biasing constant current source is connected between commonly connected sources of the first parallel connected MOS transistors and a ground reference point. A third biasing constant current source is connected between a power supply voltage source and the commonly connected drains of the second parallel connected MOS transistors, and a fourth biasing constant current source is connected between commonly connected sources of the second parallel connected MOS transistors and a ground reference point.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. **1** and **2** are system block diagrams of a two-input voltage multiplier of the prior art.

FIG. **3** is a schematic of an analog multiplier of the prior art.

FIGS. *4a–4d* are schematics of an analog function including a temperature and process compensation circuit and a voltage biasing circuit of this invention.

DETAILED DESCRIPTION OF THE INVENTION

Refer now to FIG. *4a* for a discussion of an analog integrated circuit of this invention. The analog function core circuit as described in FIG. **1**, has two differential input signals v1 and v2 that are combined according to an arithmetic function to form a differential output voltage signal vout. The magnitude of the differential output voltage signal vout is shown in EQ. 1, above.

To develop the output voltage vout, the load resistors RL1 and RL2 of FIG. *4a* are implemented as two p-type MOS transistors M5 and M6 configured to act as active load devices. The source of the active load device RL1 is connected to the inverted output (−) of the analog function core circuit and the drain is connected to the bias circuit to receive the common mode voltage Vcm. The gate is biased to a voltage level Vg, such that the active load device will operate in the linear region of the MOS device characteristics. The source of the active load device Rp2 is connected to the non-inverted output (+) of the analog function core circuit and the drain is connected to the bias circuit to receive the common mode voltage Vcm. The gate is also biased to a voltage level Vg, such that the active load device RL2 will also operate in the linear region of the MOS device characteristics.

If the analog function core circuit is implemented as the analog multiplier, as discussed above in FIG. **3**, using n-type MOS transistors, as shown, the active load devices RL1 and RL2 are implemented as the p-type MOS transistors M5 and M6 to provide compensation for changes in the currents I_{out} and I_{out2} due to fluctuations in temperature and changes in fabrication process.

The resistance of the loading devices RL1 and RL2 can be shown to be:

$$RL1 = RL2 = \frac{1}{\mu_p C_{ox}\left(\frac{W}{L}\right)_p (v_g - v_{Tp})} \qquad \text{Eq. 5}$$

where:

μ_p is the mobility of the bulk doped semiconductor material that forms the channel of the p-type MOS transistors M5 and M6.

C_{ox} is the capacitance of the gate oxide of the p-type MOS transistors M5 and M6.

$\left(\frac{W}{L}\right)$

is the width-to-length ratio of the p-type MOS transistors M5 and M6.

v_g is the voltage at the gate of the p-type MOS transistors M5 and M6.

v_{Tp} is the threshold voltage of the p-type MOS transistors M5 and M6.

The compensation circuit has an output connected to the gates of the loading devices RL1 and RL2 to provide the biasing voltage Vg to maintain the loading devices in their linear operating region. The compensation circuit further has an input terminal connected to the bias circuit to receive the common mode voltage source Vcm.

The compensation circuit, as shown in FIG. 4*b*, has a p-type MOS transistor M7 that acts as a third loading device Rp. The source of the third loading device Rp is connected to the bias circuit to receive the common mode voltage Vcm. The compensation circuit has a differential amplifier U2, with an output that provides the biasing voltage level Vg. The drain of the loading device Rp is connected to the non-inverting input (+) of the differential amplifier U2. The inverting input (−) of the differential amplifier U2 is connected to the biasing circuit that provides the a biasing voltage Vc3. The voltage level of the biasing voltage Vc3 is set between 100 mV and 200 mV lower than the desired voltage level of the common mode voltage Vcm.

The compensation circuit has an n-type MOS transistor M8 with its drain connected to the drain of the p-type loading device Rp. The compensation circuit further has a differential amplifier U1 with an output connected to the gate of the n-type MOS transistor M8.

The compensation circuit finally has an n-type MOS transistor M9 that acts as an n-type loading device Rn, with a drain connected to the source of the n-type MOS transistor M8 and the non-inverting input of the differential amplifier U1. The inverting input of the differential amplifier U1 is connected to the biasing circuit that provides a biasing voltage Vc2. The biasing voltage Vc2 is set to a voltage level of approximately 150 mV above the ground reference point. The source of the n-type loading device Rn is connected to the ground reference point. The gate of the n-type loading device Rn is connected to the bias circuit, which provides a biasing voltage Vc1.

The decoupling capacitor C_c is connected between the output terminal of the compensation circuit that provides the biasing voltage level Vg and the ground reference point. The decoupling capacitor C_c is sufficiently large to filter any high frequency noise present at the output terminal of the compensation circuit that provides the biasing voltage level Vg.

The biasing voltage level Vg at the output of the differential amplifier U2 forces the voltage level V_3 at the non-inverting input of the differential amplifier U2 to be set to the voltage level of the biasing voltage source Vc3. The current I_p is then determined as:

$$I_p = \frac{Vcm - V_3}{Rp}$$

where:

V_3 is the voltage level at the source of the p-type loading device Rp and is equal to the voltage level of the biasing voltage Vc3.

I_p is the current through the p-type loading device Rp.

Rp is the effective resistance of the p-type loading device M10 and is determined to be:

$$Rp = \frac{1}{\mu_p * C_{ox} * \left(\frac{W}{L}\right)_{p2} * (Vg - V_{Tp})}$$

where:

μ_p is the mobility of the p-type semiconductor material.

C_{ox} is the capacitance of the gate oxide of the p-type loading device Rp.

$\left(\frac{W}{L}\right)_{p2}$

is the width to length ratio of the gate of the p-type loading device Rp.

V_{TP} is the threshold voltage of the p-type loading device Rp.

As is apparent, the value of the current Ip is equal to the value of the current In through the n-type loading device Rn. The current In is determined as:

$$I_n = \frac{V_n}{Rn}$$

where:

V_n is equal to the voltage level of the biasing voltage Vc2.

Rn is the resistance of the loading device and is determined as:

$$Rn = \frac{1}{\mu_n * C_{ox} * \left(\frac{W}{L}\right)_n * (Vc1 - V_{Tn})}$$

where:

μ_n is the mobility of the n-type semiconductor material.

C_{ox} is the capacitance of the gate oxide of the p-type loading device Rn.

$\left(\frac{W}{L}\right)_n$

is the width to length ratio of the gate of the n-type loading device Rn.

V_{Tn} is the threshold voltage of the n-type loading device Rn.

Therefore, the by setting the two currents Ip and In equal and solving for the voltage $Vg-V_{Tp}$ of FIG. 5 can be shown to equal:

$$Vg - V_{Tp} = \left[\frac{\mu_n}{\mu_p}\right]\left[\frac{\left(\frac{W}{L}\right)_{n2}}{\left(\frac{W}{L}\right)_{p2}}\right](Vc1 - V_{Tn})\frac{Vc2}{Vcm - Vc3}. \quad \text{Eq. 6}$$

The differential amplifier U2 will set the biasing voltage level Vg to the voltage necessary to force the voltage level V_3 to equal the voltage of the biasing voltage level Vc3.